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DRAWINGS ATTACHED

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(54) PRODUCTION OF CIRCUIT BOARDS

(71) We, INTERNATIONAL BUSINESS MACHINES CORPORATION, a Corporation organized and existing under the laws of the State of New York in the United States of America, of Armonk, New York 10504, United States of America (assignees of ALEXANDER JOSEPH MCPHERSON and HERMAN CARL SCHEER), do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

The present invention relates to the production of circuit boards, in particular multilayer circit boards.

In the continuing effort to further reduce the size of multi-layer printed circuit panels, the problem of interconnecting layers becomes more difficult. The former method of making circuit lands where desired and then drilling holes for inserted conductor pins is not used for the smaller circuits because of the extreme difficulty in drilling the holes and reliably interconnecting the pins to the desired layers. The generally accepted method for the miniature circuits is to build up a multi-layer package by adding the interconnecting pins and layers of circuit lines sequentially.

The construction of the vertical interconnections and the layers of circuit lines may be done by either of two processes. One process is to selectively expose photo-resist on a layer of conductive material, usually copper, then develop the resist and selectively etch the metal to leave the circuit lines or pins where desired. The remaining photo-resist is removed and the etched areas are then filled by pressing an insulative material onto the surface; thereafter insulation is removed from the top of the lines. Another layer of metal is added to the lines and the photo-resist and etching steps are repeated for the next layer of circuits or pins. Successive layers of pins or lines are added similarly.

A second process is to form circuit lines on a substrate, as by etching or screening, and then applying an insulative paste, such as a curable resin, to selected areas. Portions of the circuit lines beneath the resin are left exposed for construction of the pins. A thin layer of conductive material is coated over the entire upper surface of insulation, and exposed circuit lines and portions of the conductive material are masked. The unmasked portions are then built up by electroplating. A second circuit layer is formed by unmasking portions of the conductive material in the form of circuit lines and continuing build up. The mask is removed and the conducting material not plated is etched away. Most of the circuit lines and pins are formed by plating so that the latter method is an additive process.

The characteristics of the known subtractive processes seriously limit the degree of miniaturization obtainable. A primary drawback is the difficulty in controlling the undercutting and uniformity of the etchant for fine lines. A second disadvantage is the pressed application of sheet insulator which tends to fracture pins or circuit lines. Voids can occur near the edges of the lines and pins because the insulation does not readily flow. This adversely affects circuit impedance. In addition, metal is wasted and numerous etchant and rinse baths are required.

The additive processes overcome several of the disadvantages of subtractive techniques. The line and pin resolution is limited only by that obtainable by the exposure and development of the photo-resist. Hence finer line and pin size is possible. These processes conserve metal and also reduce the number of treatment baths. The problem of undercutting is eliminated and the number of glass exposure masters may be reduced.

The known additive processes, however, still possess the difficulty of emplacing the insulation required between layers. The screening or spraying techniques proposed for a paste require relatively large openings because of the irregular edges at the holes. When forming pins of greater than approximately .030 inches in diameter these

techniques are adequate. However, in the smaller dimensions the circuit line or pin uniformity cannot be relied upon because of varying cross-sectional area. As the pin and line size is reduced the variations in edge irregularities become a larger and larger proportion of the cross-sectional area of the formed conductor. As a result the electrical resistance and pin strength are not uniform and are unreliable. The production yield is correspondingly low so that costs mount significantly.

The object of the present invention is to provide an improved process for the production of circuit boards, in particular multilayer circuit boards, and to circuit boards produced by the process.

According to the present invention a process for producing a circuit board comprises the steps of coating a substrate with a layer of electrically conducting material, selectively coating portions of said layer with spacing material, building up on the exposed portions of said conducting layer to the level of said spacing material with electrically conducting material in order to form electrically conducting regions in the spaces between said spacing material, removing all said spacing material and the portions of said conducting layer covered thereby, filling the gaps between said conducting regions with an electrically insulating material in a form having fluid properties as herein defined, hardening said insulating material and removing excess insulating material in order to expose fully the surfaces of said electrically conducting regions.

A material having fluid properties is defined as a material in powder or liquid form.

According to another aspect of the invention a process for producing multi-layer circuit boards comprises repeating the above process using the composite layer of the electrically conducting regions and the hardened electrically insulating material as said substrate.

The invention also comprises a circuit board or multi-layer circuit board made by either of the above processes.

In order that the invention may be more readily understood reference will now be made to the accompanying drawings, in which:

Figures 1 to 6 illustrate steps in a process for producing circuit boards in accordance with the present invention; and

Figure 7 is a sectional view of a multilayer circuit board as produced by the process illustrated in Figures 1—6.

Referring to Figure 1, a suitable insulative substrate 10 of glass cloth-epoxy resin or ceramic is "flash" coated with an electrically-conductive material 11 such as copper. A "flash" coating of metal can be formed by well-known electroless deposition methods to provide a layer a few microns thick. Steel of any variety provided it has a high enough impedance may also be used as a substrate with a thin electrolytically deposited metal to act as a separating layer. The separating layer can be removed by a "flash" etch at the end of the process. This layer establishes a temporary electrical circuit to all potential circuit points on the substrate surface.

A photo-sensitive resist coating 12 is next applied. The photo-resist may be any of those commercially available. Application is usually made by brushing, spin-coating or dipping. A preferred photo-resist, however, is "Riston" (Registered Trade Mark) a commercial product of E. I. DuPont de Nemours Co. "Riston" is available in sheet form in various thicknesses and is laminated to the plated metal 11. Two or more thicknesses can be successively laminated to provide the required thickness. The thickness of the applied photo-resist is determined by the circuit line thickness or pin height desired.

The photo-resist is exposed to light through a mask to expose areas 13 which are to be cross-linked and left in place as a protective coating during metal deposition. Areas 14 are unexposed and, upon developing, the photo-resist is removed leaving the thin metal layer 11 uncovered in those areas which are in the configuration of circuit lines and pins to be built up. It should be noted that infrared-sensitive resists may also be used. The photo-resist process description applies to "negative" type photo-resists. When "positive" type photo-resists are used, the light breaks down the resist to give reverse patterns.

After the exposed photo-resist has been developed, conductive material 15, such as copper, is added to layer 11, as shown in Fig. 2. Metal deposition is preferably done by electroplating. Conductive layer 11 serves as one electrode during electroplating so that all areas not covered with photo-resist are built up simultaneously. The photo-resist serves also as a plating resist. Metal deposition continues until the desired level is attained, usually to the top of resist layer 12. In Figs. 2—7, the electrolessly plated layers are shown as distinguishable from electroplated layers only for purposes of illustration. Such is not the case in actuality if like metals have been deposited.

The remaining photo-resist is removed at the conclusion of electroplating. Generally, immersion in a solvent, combined with brushing will remove the exposed resist. At times it may be necessary to use ultrasonic agitation. After removing the photo-resist, the substrate is momentarily dipped in an acid etchant to remove metal layer 11 in areas 13 where the photo-resist had been during plating. The etchant also attacks the

electro-deposited metal but very little metal is removed because of the relatively short time required to erode layer 11. Fig. 3 illustrates the substrate and circuits at this point.

A fluid or powdered insulative material 16 is added after the "flash" metal layer has been removed and is shown in Fig. 4. The dielectric is preferably an organic thermosetting or thermoplastic resin in either the liquid, uncured state or in a powdered, semicured B-stage. Epoxy resin has been found well-suited to this procedure. The fluid state of the resin permits the dielectric to readily flow by gravity around the circuit lines without need of pressure. The dielectric is preferably brought to a level sufficient to cover the circuit elements. This helps to insure that each element is surrounded with insulation.

Another dielectric material with suitable characteristics is powdered glass of low sintering temperature, such as a borosilicate. The glass power is applied in quantity sufficient to cover the circuit elements and then sintered at a temperature, such as 700—850° C. to form a solid mass.

The substrate with insulative material in place is placed in an oven to cure or sinter the dielectric to a solid homogeneous layer as shown. Circuit lines and pins are exposed at the top by removing the excess dielectric. Removal can be accomplished by abrading such as sanding and polishing or by shearing such as microtoming. The methods should be effective to clean the metal surfaces sufficiently to permit good contact with the next applied metal layer. If found necessary, a brief chemical etch can be used to prepare the surfaces of the circuit elements. Glass covering the circuit elements is removed by abrading or lapping.

The dielectric surface can be treated to enhance adhesion of the next conductor layer by any conventional micro roughening method such as vapor blasting, bead-blasting, etc. Adhesion can also be increased by inclusion of micro size particles in the surface which cause better bond strength by mechanical means or improved chemical bond. Removal of micro size inclusion particles from the surface by chemical means such as leaching will increase mechanical bonding.

The second layer of circuit elements is added to the first by using the same sequence of steps. In Fig. 5 the "flash" layer 17 of copper has been electrolessly plated to the top of the first layer of deposited elements 15 and cured resin 16, as shown in Fig. 4. The cured resin is preferably micro-roughened to permit good adhesion of the electrolessly applied metal. A layer of photo-resist 18 has been applied thereafter and exposed at areas 19.

As seen in Figure 6, circuit elements 20 are electrolytically plated up in those areas where the unexposed photo-resist is removed during development. Exposed photo-resist is then removed and the layer 17 is briefly etched as described above. Liquid or powdered resin 21 or glass is added and cured to complete the second layer.

Figure 7 illustrates several layers built up successively according to the method of the invention. Note that circuit pins or lines can be started or terminated where desired among the layers. Quality inspection and testing can be done at any layer of circuit elements, and, if found defective, the layer can be repaired or removed and replaced.

The step of using fluid or powdered dielectric is particularly advantageous because it eliminates the use of pressure heretofore required to push the semi-solid dielectric around the circuit elements. The pressure often resulted in fracture of the elements having a diameter of a few thousandths of an inch. The fluid dielectric readily flows into sharp corners and edge irregularities thus providing uniform impedance and offering improved support for the circuit panel.

WHAT WE CLAIM IS:—

1. A process for producing a circuit board comprising the steps of coating a substrate with a layer of electrically conducting material, selectively coating portions of said layer with spacing material, building up on the exposed portions of said conducting layer to the level of said spacing material with electrically conducting material in order to form electricaly conducting regions in the spaces between said spacing material, removing all said spacing material and the portions of said conducting layer covered thereby, filling the gaps between said conducting regions with an electrically insulating material in a form having fluid properties as herein defined, hardening said insulating material and removing excess insulating material in order to expose fully the surfaces of said electrically conducting regions.

2. A process as claimed in claim 1 in which said electrically insulating material is applied in powder form and is subsequently heated and cured in order to be hardened.

3. A process as claimed in claim 1 in which said electrically insulating material is applied in powder form and is subsequently heated and sintered in order to be hardened.

4. A process as claimed in claim 1 in which said electrically insulating material is applied in liquid form and is subsequently heated and cured in order to be hardened.

5. A process as claimed in any one of the preceding claims in which said spacing material is a photo sensitive material which is first coated over all said conducting layer and is then selectively exposed and developed

in order to be left only on portions of said conducting layer.

6. A process for producing a circuit board substantially as described with reference to Figures 1, 2, 3 and 4 of the accompanying drawings.

7. A process for producing a multi-layer circuit board comprising repeating the steps of the process as claimed in any one of the preceding claims using the composite layer of the electrically conducting regions and the hardened electrically insulating material as said substrate.

8. A process for producing a multi-layer circuit board substantially as described with reference to Figures 1, 2, 3, 4, 5 and 6 of the accompanying drawings.

9. A circuit board produced by a method claimed in any one of the preceding claims 1 to 6.

10. A multi-layer circuit board produced by a method as claimed in claim 7 or claim 8.

11. A multi-layer circuit board substantially as described with reference to Figure 7 of the accompanying drawings.

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Agent for the Applicants.

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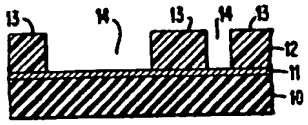

FIG. 1

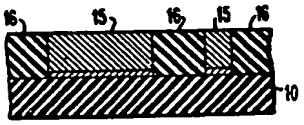

FIG. 4

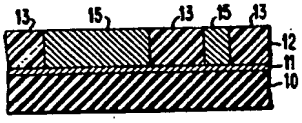

FIG. 2.

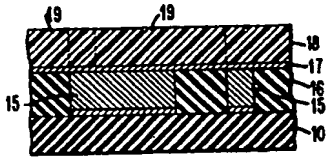

FIG. 5

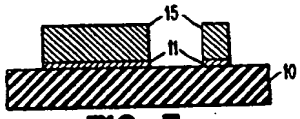

FIG. 3

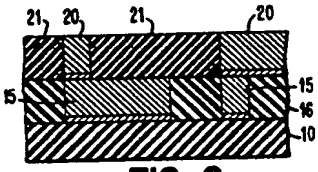

FIG. 6

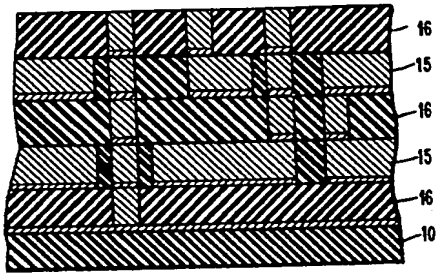

FIG. 7